time in which to reply, a response is due by 3/16/2004. This response is being filed on or before 3/16/2004, therefore, this response is being timely filed.

Remarks

As requested in paragraph 2 of the Office communication, applicants have enclosed herewith a copy of the following item referred to in the specification:

ARM Architecture Reference Manual, Version B (et. Seq.), 26 July 1996, pp 2-1 to 2-10.

In paragraph 3 of the Office communication, the Examiner requested a description of the specific improvements of the subject matter in claims 1-32 over the disclosed prior art and the specific elements in the claimed subject matter that provide those improvements. Applicants' response follows.

With regard to the prior art, during normal microprocessor operation, exceptions arise when there is a need for the normal flow of program execution to be broken, for example, so that the processor can be diverted to handle an interrupt from a peripheral. The processor state just prior to handling the exception must be preserved so that the original program can be resumed when the exception routine has completed. Many exceptions may arise at the same time.

Microprocessors of the type commonly referred to as ARM® processors, handle exceptions (interrupts) by making use of banked registers to save the processor state. These processors separate interrupt handling into discrete instruction streams, i.e., one for IRQs (Interrupt Requests) and another for FIQs (Fast Interrupt Requests). The ARM® architecture generally contemplates that FIQs are to be used for relatively high priority interrupts, and are thus provided with a higher priority than IRQs, which permits them to interrupt the processing of a pending IRQ exception call. In practice, however, it has been found by the inventors of the present invention that users often use FIQs as a part of a multi-tiered interrupt system usable by the OS. Disadvantageously, such use often results in complex nested interrupt stacks which the OS has difficulty, or is unable, to 'unwind' and properly process these interrupts. As a result, the OS is often unable to support calls from both IRQ and FIQ devices.

The present invention addresses this problem by providing a method and system for providing a single interrupt instruction stream for multiple (e.g., IRQ and FIQ) exceptions.

For example, an embodiment of the present invention shown in Fig. 2, includes a single instruction 20, which serves to simultaneously disable both FIQs and IRQs upon receipt of an IRQ exception. This instruction 20 is inserted at IRQ vector address 12. Thus, upon receipt of an IRQ, i.e., when the PC branches to IRQ vector 12, the instruction 20 disables any subsequent interrupts (both IRQ and FIQ) by setting conventional "I" and "F" bits.

This embodiment of the present invention also includes a branch instruction 22, which instructs the processor to branch to an address of a common dispatcher 24. Instruction 22 is placed at FIQ vector address 14 of the exception table 10. As shown, the IRQ vector address 12 precedes the FIQ vector address 14 in conventional ARM® exception vector tables. As such, absent a branch instruction or other exception, such as a reset, instruction execution will generally advance from address 12 to address 14.

After executing the first inserted instruction 20 located at vector address 12, execution falls through to the next instruction address, which in the embodiment shown, is at FIQ vector address 14. Branch instruction 22 previously inserted at this address 14 then instructs the processor to branch to common dispatcher 24.

Alternatively, in the event an FIQ exception 13 is received, the PC will branch directly to FIQ address 14, which in turn, will branch to the common dispatcher 24.

This embodiment of the present invention thus effectively provides a common, or merged, instruction stream at dispatcher 24 for both IRQ and FIQ interrupts. Common dispatcher 24 may process the interrupt itself, e.g., to function as a single stack interrupt handler. Additionally or alternatively, dispatcher 24 may identify the source of the exception (FIQ or IRQ) by examining the Current Processor Status Register (CPSR) mode bits. Once this determination has been made, dispatcher 24 may appropriately branch to either FIQ handler 18' or IRQ handler 16' for further processing in a conventional manner.

Advantageously, this embodiment of the present invention provides a single interrupt stream for both IRQ and FIQ exceptions, to prevent the prior art occurrence of IRQ exception handling being interrupted by FIQ exceptions. This advantage is particularly apparent in environments in which a single interrupt stack is required. The invention also advantageously permits both the FIQ and IRQ external inputs (not shown) of the ARM® processor to be used

by the operating system. This enables users, such as manufacturers of embedded applications, to utilize both IRQ and FIQ pins of ARM® processors, to potentially reduce parts count for advantageous cost savings.

CONCLUSION

Applicant submits that all of the required information has been provided, and that this application is believed to be in condition for allowance, and such action at an early date is respectfully requested. However, if any matters remain unresolved, the Examiner is encouraged to contact the undersigned by telephone.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-0374** referencing docket no. 1109.005(2000.021). However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

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